WHAT IS CLAIMED IS:

1. A precoder comprising:

a judgment unit for judging whether an odd number or even number of '1's exist in

5   data input signals of N channels inputted at an nth time of channel input;

a toggle unit for toggling an output signal of the judgment unit when said number

of '1's is judged by the judgment unit to be odd, said toggling determining an output value

of a channel of the N channels; and

communicatively connected to the toggle unit, an output unit for determining

10   output values of other channels of the N channels according to respective ones of the data

input signals.

2. The precoder as claimed in claim 1, wherein the judgment unit includes a

plurality of exclusive OR gates connected to each other in a pyramid configuration, so that

15   the judgment unit outputs to the toggle unit '0' when said number of '1's is judged by the

judgment unit to be even, or '1' when said number of '1's is judged by the judgment unit to

be odd.

3. The precoder as claimed in claim 2, wherein the output unit includes N-1 XOR

20   gates for sequentially performing an XOR operation that has as an input a respective one of

said input signals and that has as a further input a signal representative of a respective one

of the channel output values.

4. The precoder as claimed in claim 3, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising

5   edge of the output signal of the AND gate.

5. The precoder as claimed in claim 2, wherein the output unit includes N-1 XOR gates for performing XOR operations, each operation having as an input a respective one of said input signals and further having as an input a signal representative of a respective one

10   of the channel output values.

6. The precoder as claimed in claim 5, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock signal; and

15   a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising edge of the output signal of the AND gate.

7. The precoder as claimed in claim 2, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock

20   signal; and

a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising edge of the output signal of the AND gate.

8. The precoder as claimed in claim 1, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising

5 edge of the output signal of the AND gate.

9. The precoder as claimed in claim 1, wherein the output unit includes N-1 XOR

gates for sequentially performing an XOR operation that has as an input a respective one of

said input signals and that has as a further input a signal representative of a respective one

10 of the channel output values.

10. The precoder as claimed in claim 9, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising

15 edge of the output signal of the AND gate.

11. The precoder as claimed in claim 1, wherein the output unit includes N-1 XOR

gates for performing XOR operations, each operation having as an input a respective one of

said input signals and further having as an input a signal representative of a respective one

20 of the channel output values.

12. The precoder as claimed in claim 11, wherein the toggle unit comprises:

an AND gate for ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) for toggling an output signal of the AND gate at each rising
5   edge of the output signal of the AND gate.

13. A precoder for coding data input signals of N channels inputted at an nth time of channel input, said precoder operating according to the equations:

$$b_{Nn+1} = a_{Nn+1} \oplus b_{Nn}$$
$$b_{Nn+2} = a_{Nn+2} \oplus b_{Nn+1}$$
$$b_{Nn+3} = a_{Nn+3} \oplus b_{Nn+2} \quad ,$$
$$\ldots$$
$$b_{Nn+N} = a_{Nn+N} \oplus b_{Nn+(N-1)}$$

10   wherein a_{Nn+k} represents input data of an kth of said N channels, b_{Nn+k} represents

an output signal of the precoder for the kth of said N channels, and $\oplus$ represents an

exclusive OR operation.

14. The precoder as claimed in claim 13, wherein the precoder comprises:
15   N number of XOR gates for receiving the data signals a_{Nn+1} to a_{Nn+N}, respectively;

and

a delayer connected to an output terminal of an Nth XOR gate,

wherein an output signal of the delayer is fed back to a first one of the N gates, to

which the data signal a_{Nn+1} is inputted.

15. The precoder as claimed in claim 14, wherein the N is 4.

16. An optical duo-binary transmission apparatus comprising:

5   a precoder for coding in parallel data input signals of N channels; and

a multiplexer for time division multiplexing the signals coded by the precoder.

17. The optical duo-binary transmission apparatus as claimed in claim 16, wherein the precoder comprises:

10   a judgment unit for judging whether an odd number or even number of '1's exist in data input signals of N channels inputted at an nth time of channel input;

a toggle unit for toggling an output signal of the judgment unit when said number of '1's is judged by the judgment unit to be odd, said toggling determining an output value of a channel of the N channels; and

15   communicatively connected to the toggle unit, an output unit for determining output values of other channels of the N channels according to respective ones of the data input signals.

18. The optical duo-binary transmission apparatus as claimed in claim 16, wherein

20 the precoder further comprises a unit to which the data input signals serve as input, said unit being comprised of m stages of XOR gates wherein $N = 2^m$.

19. The optical duo-binary transmission apparatus as claimed in claim 18, wherein the precoder further comprises an output unit having N-1 stages of XOR gates.

20. The optical duo-binary transmission apparatus as claimed in claim 19, wherein the units comprised on m stages is joined to the output unit by an AND gate feeding a T flip-flop (T-FF).